

Immunity of Operational Amplifiers against High Frequency and High Amplitude Pulse Interferences

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Abstract: The number of electronic (mobile) devices in the world is ever increasing. With this increase of transmitting devices, the electromagnetic interference (EMI) between those devices and other equipment becomes a bigger challenge. This raises the need for equipment and therefore integrated circuits that are more robust to the presence of Electromagnetic waves. In this study, the effect of radio frequency interference in operational amplifiers is dealt with by introducing a parameter to unambiguously specify the EMI robustness of an Op-Amp: EMI Rejection Ratio (EMIRR). This paper presents the background, details and usage of the EMIRR parameter in determining the sensitivity of op-amp to electromagnetic interference.

Keywords: OP –Amps, Electromagnetic Interference, EMRR. RF, Modeling, Simulation, Offset Voltage

1. Introduction

In recent years due to increasing adoption of electronic and microelectronic equipments EMI has been more and more carefully studied and experimentally evaluated in order to find possible prevention methodologies, especially in high performance digital/analog ICs which may include several operational amplifiers - Op-Amps. (Richelli, et.al, 2002) It is worth mentioning that circuits that perform analog operations are more sensitive to EMI, (Anyaoha and Osunde, 2011). Many methods have been proposed in literature for parasitic modeling, such as three dimensional finite element analysis, time-domain reflectometry and partial element equivalent circuit method. These methods are all purely mathematical and developed based on computer simulation, and thus are very time consuming, because the circuit models are very complicated.

Another fundamental limitation of these methods is that expensive instrument and sophisticated simulation tools are mandatory. Disturbing processes are generally studied and analysed relating to EMC. If they relate to op-amps, which have nonlinear elements on their inputs and outputs, they become so complicated, that the only suitable technique to study and analyze them is numerical modeling or simulation. This operation is straightforward for linear systems, but rarely usable for modeling of nonlinear processes, which are considered as a reason of influencing the function of analog electronic circuits by impulsive disturbance. It means that for modeling of EMC behavior of op-amps, models having partial bordering elements submodels must be

used. Therefore the detailed structure of op-amps I/O circuits must be known and precisely modeled according to Hallon et.al (2002).

In order to investigate the EMI immunity level it is good to measure it in the voltage follower configuration. It is quite easy to understand why the voltage follower topology represents the worst case: in this configuration Richelli, et.al (2001) asserted that due to direct connection between the output and the inverting input node, the gates of the differential pairs experience the largest voltage difference.

In 2000, an updated version of the integrated circuit Electromagnetic immunity Handbook published by NASA gave valuable information on the immunity levels of simple integrated circuits up to 10GHz.

Further investigations have also been concerned with nonlinear model of EMI-induced distortion in feedback CMOS operational amplifiers. It takes into account distortion phenomena induced by RFI in the differential pair transistors only. In particular, the input offset voltage induced by Continuous Wave (CW) RFI superimposed on the input nominal signals of feedback CMOS op-amps is derived by evaluating the mean-value of the current flowing in the two branches of the input differential pair.(Fiori2002)

Another investigation was carried out on the canonical Resistance Inductor diode (RLD) circuit modeling the nonlinear dynamic of a p-n junction, along with a trans impedance amplifier (TIA), and found a striking change in the onset of period – doubling under RF stimulus, Moraes et.al (2002)



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show that high RF power enhances the nonlinear and chaotic behavior at lower LF voltages for the RLD-TIA circuits. Besides p-n junction and TIA, investigations have also been focused on PWM controllers for SMPS and it has been shown that the switching activity of power transistors modulates the amplitude of RF interference added to nominal IC signals and the amplitude of the substrate RF voltage bounce. As consequence, RF susceptible circuits, which are included in the DUT, demodulate such interference and the nominal operation of the overall system is modified. In the specific case of smart power IC, which operate in feedback control system, it has been shown by Friori (2003) that the simultaneous presence of switching power transistors and EMI-induced non linear phenomena in analog control circuits, activate a low frequency parasitic feedback that strongly influence the nominal behavior of the overall system.

It is well known that one of the most susceptible circuits to RF noise is the operational amplifiers. One of the undesirable effects of interference is a shift of the output DC mean value (DC offset) that might force the amplifier, or subsequent stage into saturation. The susceptibility of these circuits is highlighted in several studies. Jovic (2010) and Hallon et.al (2003).

Similarly, analysis is also done on prediction of RF interference in op-amps by a new analytical method. This model gives a rigorous justification of the main cause of even order distortion in integrated differential pairs. Although this model is not suitable to study the behavior of operational amplifiers in the presence of very high amplitude disturbances, as it is based on the assumption that all the devices work in their nominal region of operation, it provides a good insight in the phenomenon and, especially, relates it to design parameters and parasitic. These features make the proposed approach suitable in order to derive low RFI design criteria and to develop new high immunity structures as well, (Fiori et.al 2001).

In section 2, the procedure for RF injection experiment will be discussed in detail and in section 3 results of measurement. Analysis of results is presented in section 4 and in section 5, conclusion.

2 RF Injection Experiment

Direct injection and irradiation experiments are the two types of experiments commonly used for determining the effects of electromagnetic radiation in electronics. Direct injection experiments have the advantage of being able to couple the most power into a specific point in a circuit, to exactly know how much power is incident to the device under test, but has the disadvantage of creating a fictitious circuit environment to determine the effects. Irradiation

experiments have the advantage of not altering the circuit under test and keeping the integrity of the circuit testing environment as ideal as possible. The disadvantages of irradiation include the requirement for higher power levels, antenna patterns changing with frequency, near-field ambiguities, and difficulties in calculating the exact amount of power incident to a circuit or transmission line.

Direct injection experiments were chosen so that the frequency of the injection signal can be easily determined and also it will be possible to inject the RF signal in the exact pin under test. This method can be used to measure precisely how much power is incident to, reflected from and transmitted into the DUT. By using a power coupler, the incident and reflected RF power is measured and the transmitted power calculated from these values. However, this setup can incorporate an unrealistic circuit environment due to loading effects at the injection point. As a consequence a virtual circuit and apparatus are used for the analysis (Multisim 10.0)

2.1 EMIRR Measurement

Measuring EMIRR is straightforward and requires three basic actions:

1. Applying an RF signal in a well defined way to an op amp pin under test.
2. Measuring the offset voltage with the RF signal switched off and again with the RF signal switched on.
3. Calculate the resulting offset voltage shift from which the EMIRR can be obtained.

The three steps stated above will be implemented with multism

$$\Delta V_{offset} = V_{offset} \cdot 10^{EMIRR/20} \quad (1)$$

Since the standard RF peak voltage is 100mV it follows that equation (1) now becomes

$$\Delta V_{offset} = V_{offset} \cdot 10^{EMIRR/20} \quad (2)$$

Equation (2) is the standard form of calculating EMIRR, other values of EMIRR can be obtain as follows

$$\Delta V_{offset} = V_{offset} \cdot 10^{EMIRR/20} \quad (3)$$

$$\Delta V_{offset} = V_{offset} \cdot 10^{EMIRR/20} \quad (4)$$

For example assume $EMIRR_{1V}$ is measured for an op-amp converting to the standard yields

$$EMIRR_{1V} = \frac{20 \cdot \log \left(\frac{\Delta V_{offset}}{V_{offset}} \right)}{10^{-1}} \quad (6)$$

In order to obtain a defined RF levels on the pin under test, no op-amp feedback elements should be in the RF signal path. Therefore, if possible, the op amp should be connected in a unity-gain configuration. This yields the lowest level of RF filtering due to the feedback network. Figure 1 shows the circuit diagram for connecting the RF signal to the non inverting

terminal. The behavior of the output voltage was recorded. A unity gain configuration was used for this stage.

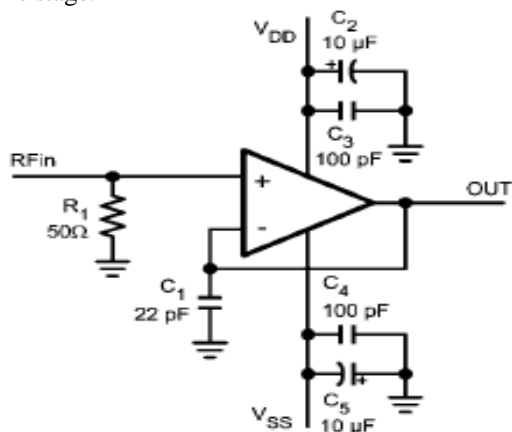


Figure 1 Circuit Diagram for injecting RF signal to the non - inverting pin

When the pin under test is tested, the other pins need to be decoupled for RF signals. This ensures that the obtained offset voltage shift is dominantly a result of coupling the RF signal to the pin under test. For this decoupling standard components can be used.

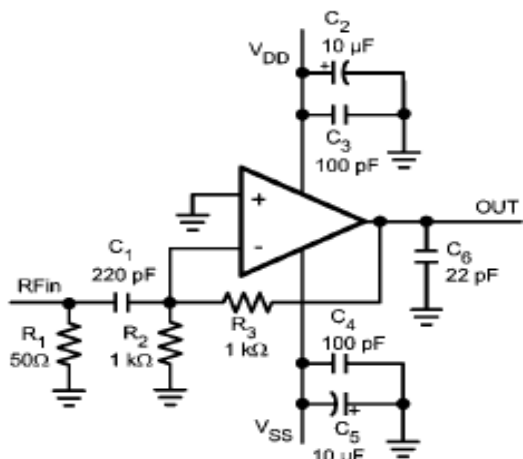


Figure 2 Circuit diagram for injecting RF signal to the inverting pin

For coupling an RF signal to the inverting pin, the unity gain configuration as described for the non inverting pin will not work. In that configuration the RF signal would be applied not only to the inverting pin but to the output pin as well. For accurately measuring the EMIRR of the inverting pin, RF isolation is required for the output pin. Therefore a voltage gain configuration is used as depicted in figure 2 the low-frequency gain, which applies to the resulting offset shift, is set to 2. The feedback resistor R_3 and the load capacitance isolate the output pin from the injected RF signal at the inverting pin.

The RF signal is applied to the inverting pin via a coupling capacitor C_1 . The parasitic series inductance of this capacitor needs to be compared to the 50Ω impedance of the RF signal path. So, an inductance of a few nH is acceptable when measuring up to a few GHz. For symmetry reasons it is expected that the positive and negative input have the same sensitivity for applied RF signals but with an opposite polarity for the obtained input referred offset shift. The input pins thus have the same EMIRR

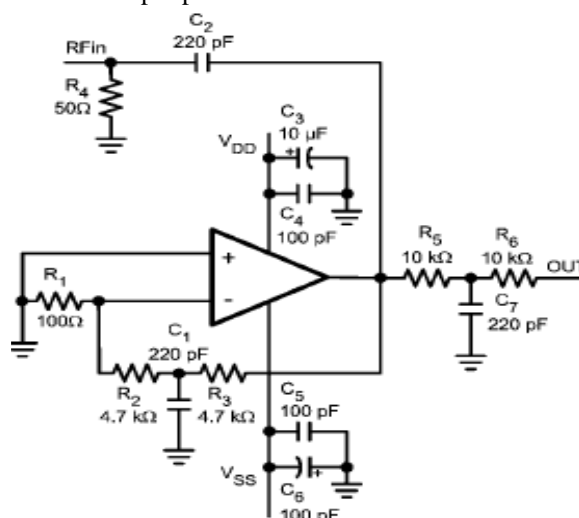


Figure 3 Circuit diagram for injecting RF signal to the output pin

Analogous to the circuit for testing the inverting pin, the circuit for testing the output pin requires a voltage gain configuration. When applying an RF signal to the output pin, the inverting pin needs to be isolated. As the sensitivity of the output pin is expected to be lower than the sensitivity of the input pin, a better isolation is needed for this case. The experimental setup for coupling an RF signal to the output pin is depicted in Figure 3 The resulting offset shift is again measured at the output.

So, the equivalent input referred offset voltage shift is found by dividing the obtained output voltage shift by the gain of the configuration: $1 + (R_2 + R_3)/R_1$. Special attention needs to be paid to the isolation of the DC meter connected to the output. As the RF signal is applied to the same node where the resulting offset voltage shift needs to be measured, a low-pass filter (R_5 , R_6 , and C_7) is placed between the RF injection node and the DC meter. This low-pass filter prevents the DC meter from detecting the applied RF signal which would directly affect the measurement results

3. Measurements Result

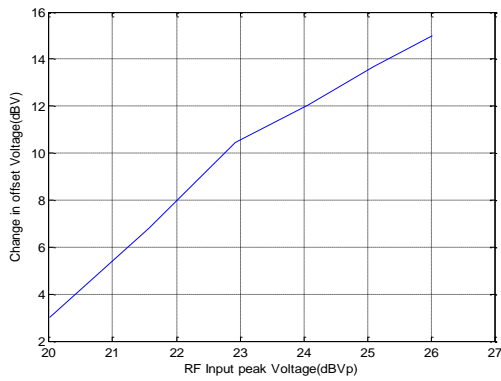


Figure 4 Graph of Measured Input referred offset voltage shift vs. Applied RF peak level for IN₊ (300MHz)

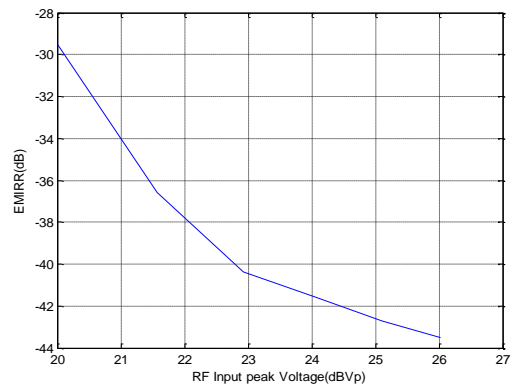


Figure 5 Graph of EMIRR vs. RF input peak level for IN₊ (300MHz)

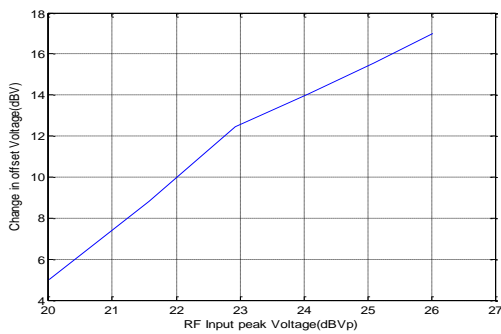


Figure 6 Graph of Measured Input referred offset voltage shift vs. Applied RF peak level for IN₊ (1GHz)

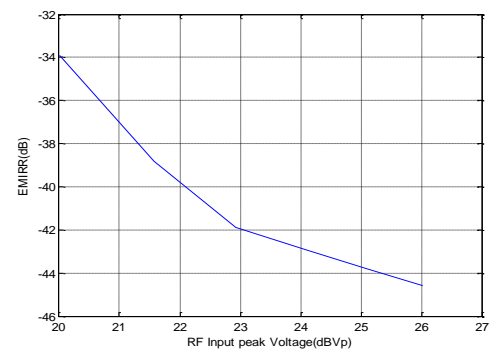


Figure 7 Graph of EMIRR vs. RF input peak level for IN₊ (1GHz)

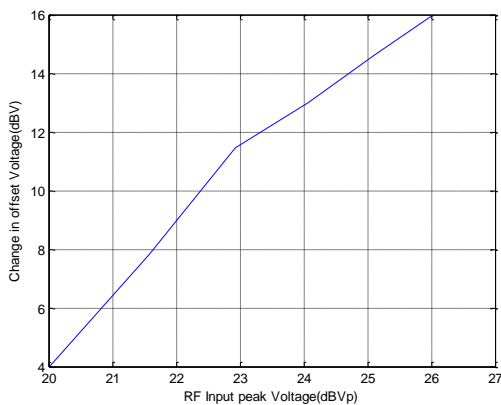


Figure 8 Graph of Measure Inputreferred offset voltage shift vs. Applied RF peak level for IN₋ (300MHz)

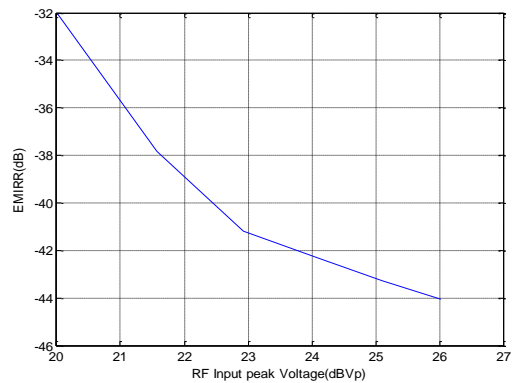


Figure 9 Graph of EMIRR vs. RF input peak level for IN₋ (300MHz)

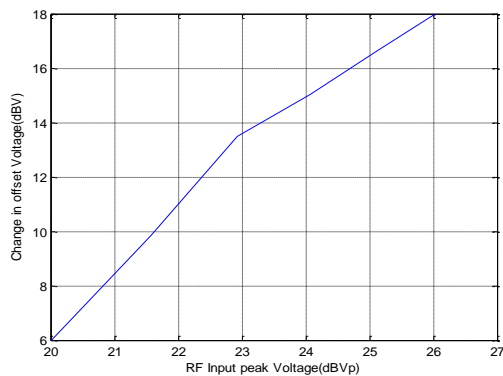


Figure 10 Graph of Measure Input referred offset voltage shift vs. Applied RF peak level for IN. (1GHz)

4. Discussion of Results

The software used in this work is Multisim 10.0.1. It provides a virtual circuit for simulation and testing. The virtual experimental circuit is as shown in figure 1-3 The op-amp behavior was evaluated for normal operation without any interference injected and the result gave a linear response of output with respect to the input as expected. From figure 4 it can be seen that the offset voltage is directly proportional to the applied RF peak voltage. When the amplitude of the RF signal increases the offset voltage also increases. From the experimental results it can be seen that the non-inverting terminal is sensitive to RF disturbances so there is the need to design the terminal to have strong immunity to RF interferences.

Considering figure 5 it can be deduce that there is inverse proportionality between the RF input peak voltage and the EMIRR. As proposed earlier in the work it could be seen that the higher the EMIRR parameter the more resistant the terminal is to Electromagnetic interference. This can be use as criteria when designing an op-amp knowing that op-amps with higher EMIRR is more robust to EMI. The result from the inverting terminal is similar to those from the non-inverting terminal. Figure 8 and 10 shows the graph of offset voltage against RF peak voltage for 300MHz and 1GHz respectively for the inverting terminal comparing it with 4 and 6 it can be seen that the graphs have approximately the same slope. This shows that the inverting and non-inverting terminal have the same sensitivity to Electromagnetic interference. Also comparing figure 5 and 7 with figure 9 and 11 it could be seen that the EMIRR varies in the same order

Finally, from the experimental results it was observed that the output terminal is more robust to EMI compare to the inverting an non-inverting but that

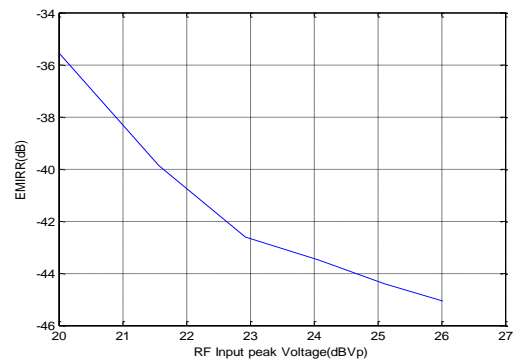


Figure 11 Graph of EMIRR vs. RF input peak level for IN. (1GHz)

does not mean that the output terminal should not be shielded against RFI.

5. Conclusions

Macromodel has been used to investigate the effects of EMI in operational amplifiers (AD8532ARM Op-amp circuit). EMI disturbances at the input and output of the op-amp circuit was investigated with the use of computer program multisim by injecting noise in form of RF to the output, inverting and non-inverting pins at a frequency of 300MHz and 1GHz. A value for determining the EMI robustness of operational amplifies was determined.

It was discovered from the graph that the IN_+ and IN_- pin do have similar EMIRR. This was already noticed for reasons of input stage symmetry. The output pin have a significantly higher EMIRR than the input pins. This is also quite logical as the inputs are meant to be sensitive for signals. It should be noted, however that the supply and output pin are not generally more robust than the input pins. An op-amp needs to be designed specifically for having high EMIRR for those pins as well. When designing equipment in a high interference region the ICs to be used need to be tested to determine their EMIRR to ensure it can withstand the interference.

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